

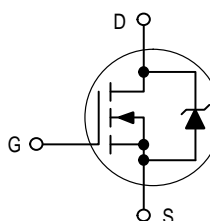
*Advance Information*

**TMOS E-FET™**

**Power Field Effect Transistor**  
**N-Channel Enhancement-Mode Silicon Gate**

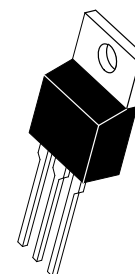
This advanced TMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters, PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$  and  $V_{DS(on)}$  Specified at Elevated Temperature



**IRF540**

**TMOS POWER FET**  
**27 AMPERES**  
**100 VOLTS**  
 **$R_{DS(on)} = 0.077$  OHMS**



**CASE 221A-06**  
**TO-220AB**

**MAXIMUM RATINGS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	100	Vdc
Drain-to-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	100	Vdc
Gate-to-Source Voltage — Continuous — Non-repetitive ( $t_p \leq 10 \text{ ms}$ )	$V_{GS}$ $V_{GSM}$	$\pm 20$ $\pm 40$	Vdc Vpk
Drain Current — Continuous — Continuous @ $100^\circ\text{C}$ — Single Pulse ( $t_p \leq 10 \mu\text{s}$ )	$I_D$ $I_{D1}$ $I_{DM}$	27 19 95	Adc Apk
Total Power Dissipation Derate above $25^\circ\text{C}$	$P_D$	145 1.16	Watts W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy — STARTING $T_J = 25^\circ\text{C}$ ( $V_{DD} = 50 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , PEAK $I_L = 27 \text{ Apk}$ , $L = 1.0 \text{ mH}$ , $R_G = 25 \Omega$ )	EAS	365	mJ
Thermal Resistance — Junction-to-Case — Junction-to-Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.86 62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

# IRF540

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 0.25 mAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	100	— 116	—	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 100 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 100 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	—	—	10 100	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	—	—	100	nAdc

### ON CHARACTERISTICS(1)

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	2.0	2.9 6.8	4.0	Vdc mV/°C
Static Drain-to-Source On-Resistance (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 15 Adc)	R <sub>DS(on)</sub>	—	0.047	0.077	Ohms
Drain-to-Source On-Voltage (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 27 Adc) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 15 Adc, T <sub>J</sub> = 125°C)	V <sub>DS(on)</sub>	—	—	2.5 2.4	Vdc
Forward Transconductance (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 15 Adc)	g <sub>FS</sub>	10	15	—	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	—	1460	2040	pF
Output Capacitance		C <sub>oss</sub>	—	390	550	
Transfer Capacitance		C <sub>rss</sub>	—	120	240	

### SWITCHING CHARACTERISTICS(2)

Turn-On Delay Time	(V <sub>DD</sub> = 50 Vdc, I <sub>D</sub> = 27 Adc, V <sub>GS</sub> = 10 Vdc, R <sub>G</sub> = 9.1 Ω)	t <sub>d(on)</sub>	—	12	20	ns
Rise Time		t <sub>r</sub>	—	105	210	
Turn-Off Delay Time		t <sub>d(off)</sub>	—	50	100	
Fall Time		t <sub>f</sub>	—	65	130	
Gate Charge (See Figure 8)	(V <sub>DS</sub> = 80 Vdc, I <sub>D</sub> = 27 Adc, V <sub>GS</sub> = 10 Vdc)	Q <sub>T</sub>	—	50	70	nC
		Q <sub>1</sub>	—	9.0	—	
		Q <sub>2</sub>	—	26	—	
		Q <sub>3</sub>	—	20	—	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage (I <sub>S</sub> = 27 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 27 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	—	0.93 0.84	1.0	Vdc	
Reverse Recovery Time	(I <sub>S</sub> = 27 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	—	110	—	ns
		t <sub>a</sub>	—	100	—	
		t <sub>b</sub>	—	10	—	
Reverse Recovery Stored Charge	Q <sub>R</sub>	—	0.67	—	μC	

### INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L <sub>d</sub>	—	3.5 4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L <sub>s</sub>	—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

(3) Reflects typical values.  $C_{pk} = \frac{|\text{Max limit} - \text{Typ}|}{3 \times \text{sigma}}$

TYPICAL ELECTRICAL CHARACTERISTICS

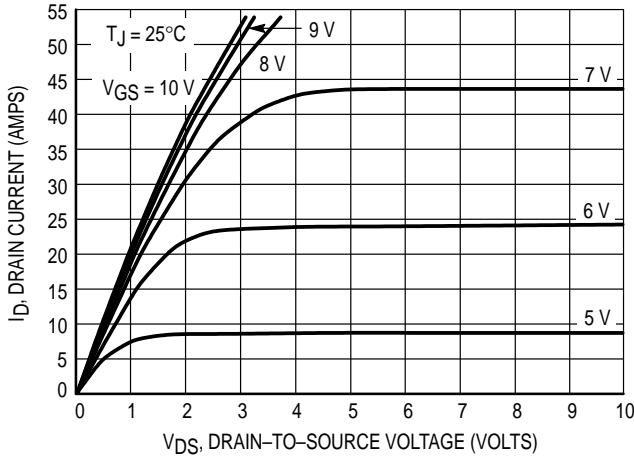


Figure 1. On-Region Characteristics

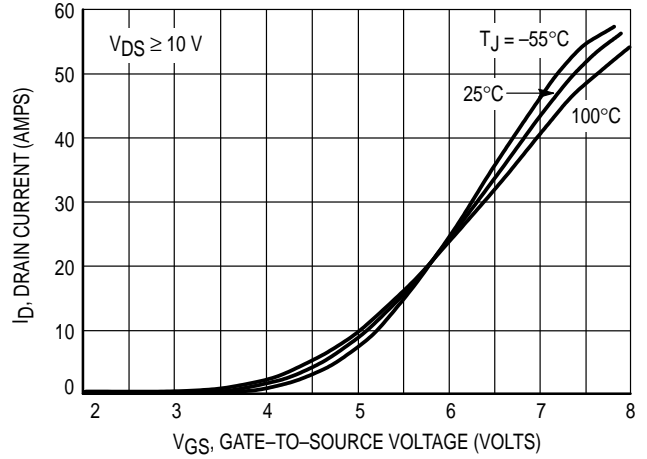


Figure 2. Transfer Characteristics

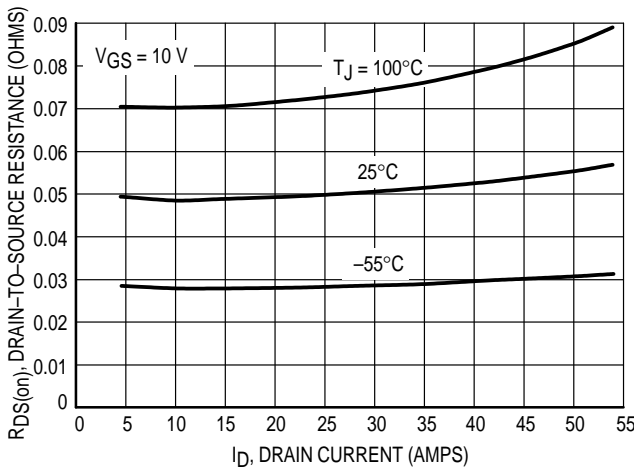


Figure 3. On-Resistance versus Drain Current and Temperature

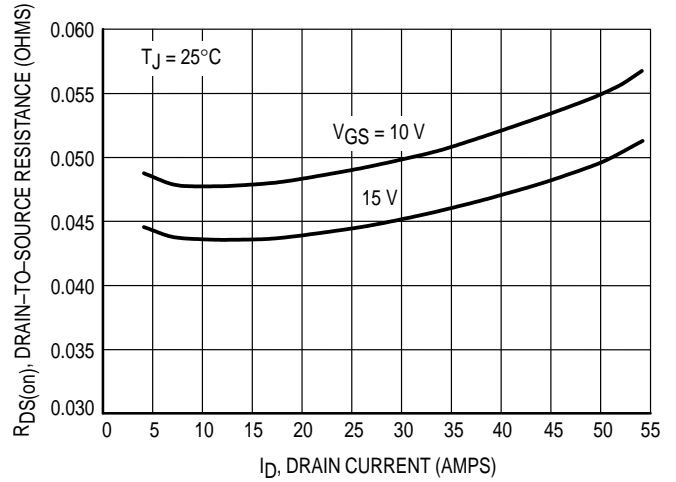


Figure 4. On-Resistance versus Drain Current and Gate Voltage

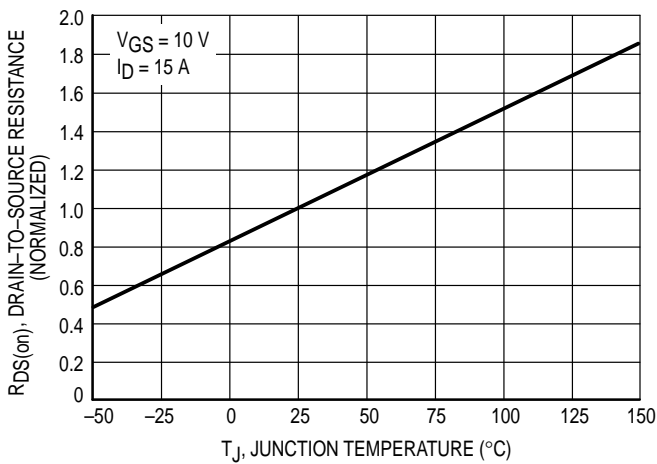


Figure 5. On-Resistance Variation with Temperature

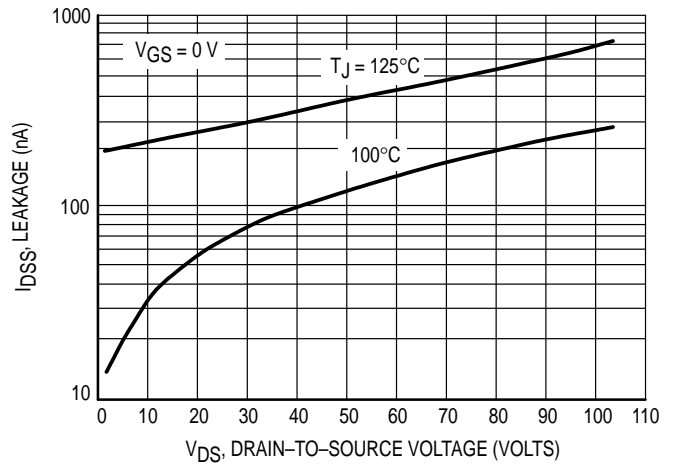


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

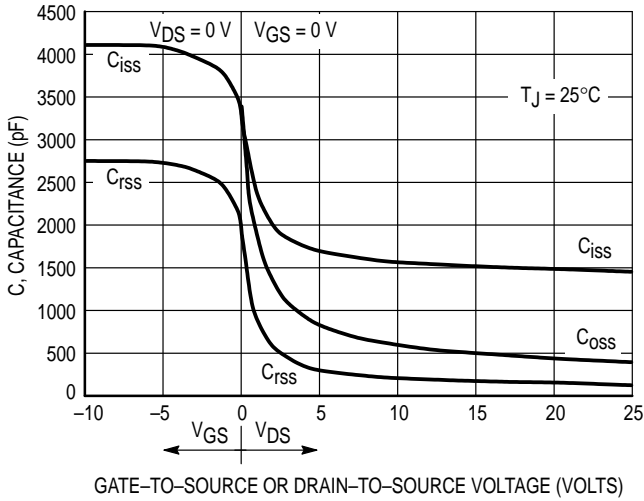


Figure 7. Capacitance Variation

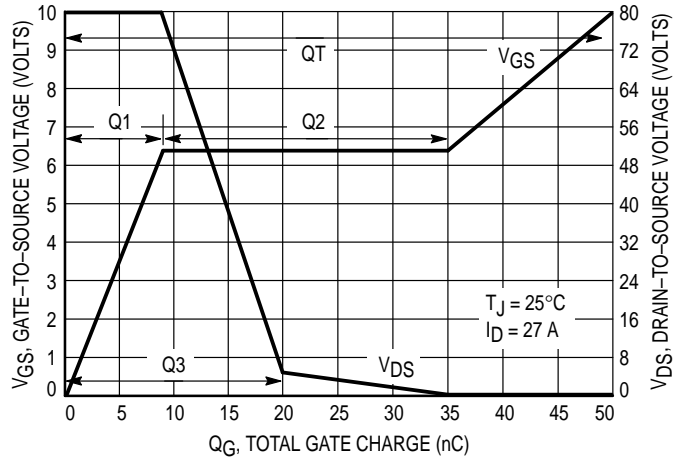


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

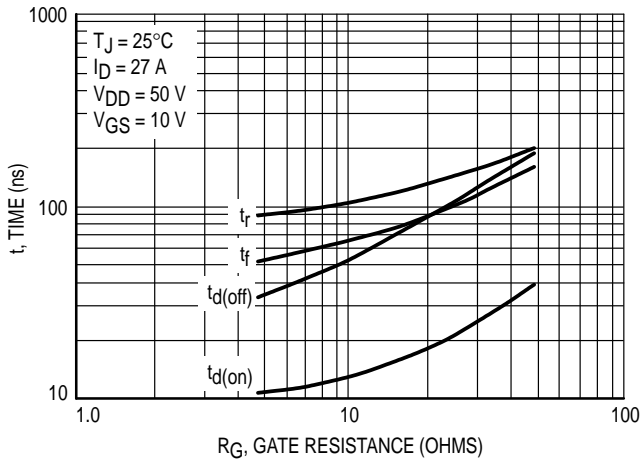


Figure 9. Resistive Switching Time Variation versus Gate Resistance

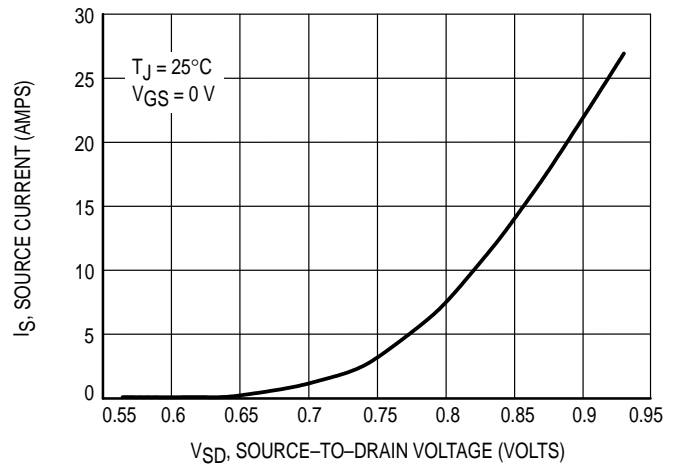


Figure 10. Diode Forward Voltage versus Current

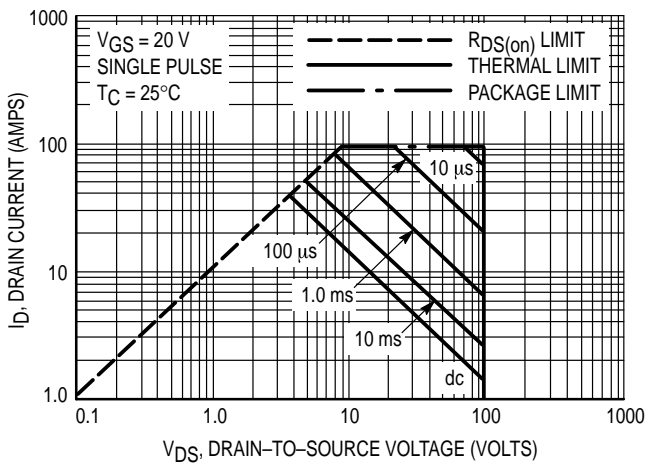


Figure 11. Maximum Rated Forward Biased Safe Operating Area

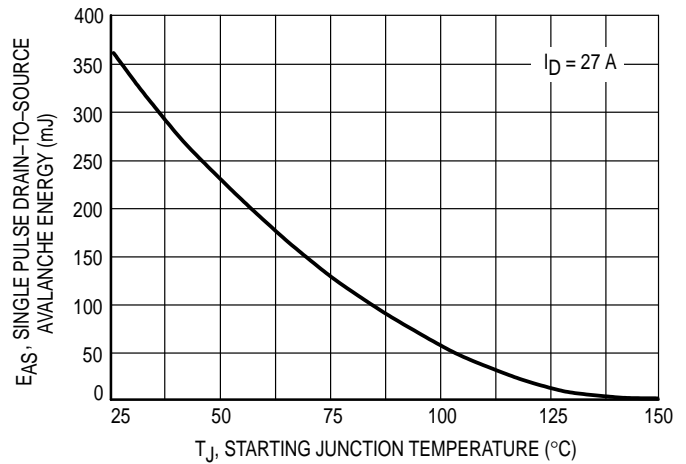


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

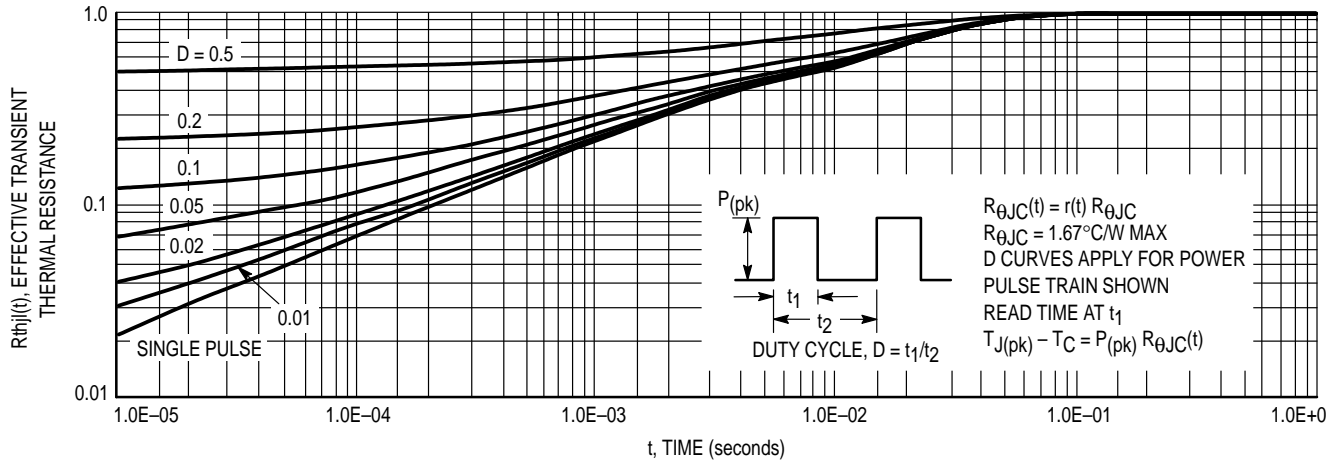
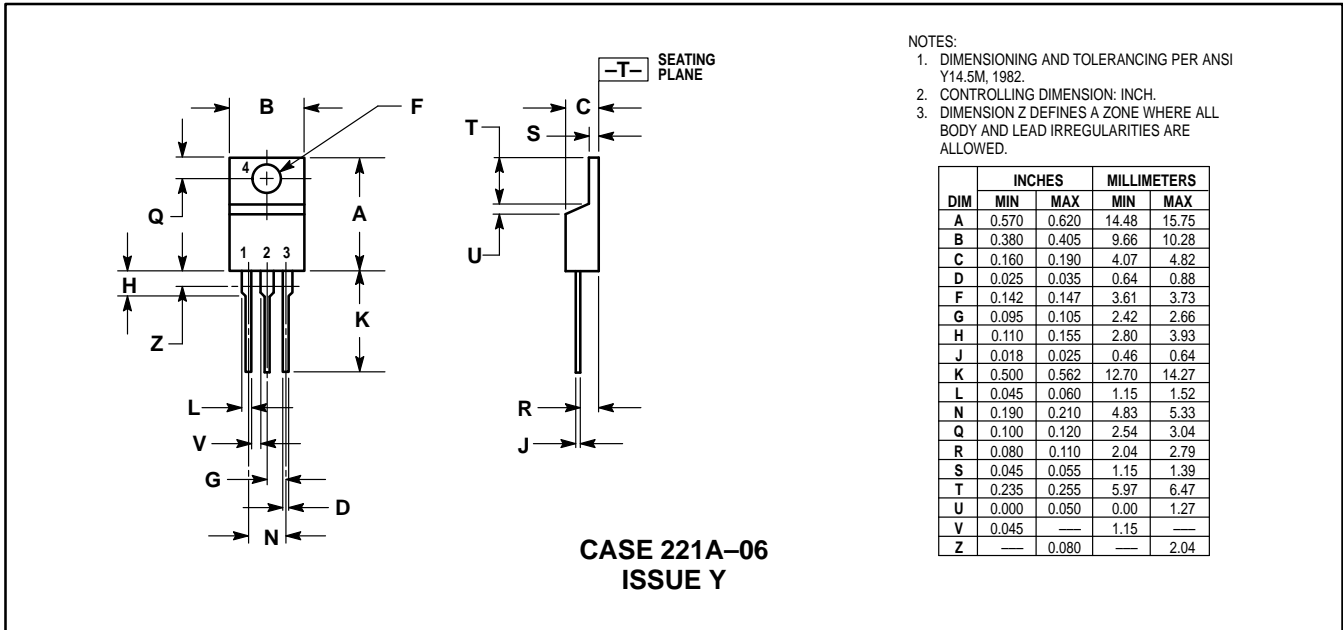


Figure 13. Thermal Response

PACKAGE DIMENSIONS



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